Amendments to the Drawings:

The attached sheets of drawings include changes to Figure 4. The attached Figure 4 replaces the original Figure 4.

Attachment: Replacement Sheet

REMARKS

Reconsideration and further examination of the present application is respectfully requested. The Office Action has rejected claims 1-9, 11-39 and 41-45. Applicants have amended claims 1, 5, 7, 11, 17, 24, 31, 35, 37, and 41. Furthermore, Applicants have canceled claims 3, 4, 6, 9, 10, 33, 34, 36, 39, and 40.

Specification

Applicants amended the typographical error in paragraph [0038] to change reference number 420 to reference number 421. Similarly, Applicants amended the typographical error in Figure 4 to change reference number 420 of the box labeled "Allocate an Additional Storage Element" to reference number 421. Applicants added no new matter through the amending of the typographical errors.

Objections to the Claims

Claims 10, 40, and 46 have been objected to as being dependent upon a rejected base claim. Applicants amended claim 1 to include the limitations of claim 10 and all the intervening claims as the office action indicates would place the claim in an allowable form. Similarly, Applicants amended claim 31 to include the limitations of claim 40 and all the intervening claims as the office action indicates would place the claim in an allowable form.

35 USC § 103

Claims 1-3, 31-33, 41, and 42 have been rejected under 35 USC 103(a) as being unpatentable over U.S. Publication No. US 2002/0154634 A1 to Basso et al ("Basso") in view of U.S. Patent No. 6,658,014 B1 to Tezuka ("Tezuka").

Claims 4 – 7, 9, 11-14, 16-28, 30, 34-37, 39, and 42-45 have been rejected under 35 USC 103(a) as being unpatentable over Basso and Tezuka as applied to claims 1 and 3 and further in view of U.S. Patent No. 4,809,269 to Gulick ("Gulick").

Claims 8, 15, 29, and 38 have been rejected under 35 USC 103(a) as being unpatentable over Basso, Tezuka and Gulick as applied to claims 1, 3, 4, 6, 7, 11, 13, 14, 24, 27, and 28, and further in view of U.S. Patent No. 6, 269,081 B1 to Chow ("Chow").

Claims 1 and 31

Claims 1 and 31 have been amended to include limitations of dependent claims as the office action indicated would put the claims in a condition for allowance.

Claims 2, 5, 7, and 8

Applicants respectfully submit that claims 2, 5, 7, and 8 are dependent directly or indirectly on claim 1, thus include the same limitations as claim 1. As such, claims 2, 5, 7, and 8 are allowable for at least the same reasons as claim 1.

Claims 32, 35, 37, and 38

Applicants respectfully submit that claims 32, 35, 37, and 38 are dependent directly or indirectly on claim 31, thus include the same limitations as claim 31. As such, claims 32, 35, 37, and 38 are allowable for at least the same reasons as claim 31.

Claim 41

Applicants respectfully submit the combination of Basso and Tezuka fails to describe or suggest each and every element of amended claim 41.

Amended claim 41 requires maintaining a transmit count value of each one of said plurality of storage elements *stored within each one of said plurality of storage elements* storing a plurality of packet data. Moreover, claim 41 requires determining a release count value of *each one of said plurality of storage elements*. Claim 41 also requires comparing said transmit count value and said release count value for each one of said plurality of storage elements.

Basso describes data structures, a method, and an associated transmission system for multicast transmissions on network processors in order both to minimize multicast transmission memory requirements and to account for port performance discrepancies. (Basso, Abstract). For multicast transmissions, Basso describes a "Multicast Counter" (MCC) used to determine when all the instances have been transmitted so that the reference frame can be discarded. (Basso, para. [0085]). Furthermore, Basso describes that the MCC is stored in a reference FCB and not in its associated buffers. (Basso, para. [0085]). Moreover, when the MCC stored in the reference FCB reaches zero, the FCB

and its associated buffers are discarded by returning them to the free FCB and free buffer queues respectively. (Basso, para. [0085]).

Therefore, the MCC is stored in a reference FCB and not in each one of said plurality of storage elements storing a plurality of packet data. As such, Basso fails to describe or suggest maintaining a transmit count value of each one of said plurality of storage elements stored within each one of said plurality of storage elements storing a plurality of packet data.

Tezuka describes a packet buffer device and a packet assembling method in a packet transfer module to assemble logical channel-multiplexed asynchronous transfer mode (ATM) cells into packets and to store and output the cells in packet units (Tezuka, Abstract). The device dynamically constructs common buffers and discrete buffers. (Tezuka, col. 3, ll. 10-12). Specifically, Tezuka describes the use of a packet length (buffer count) that is written into the transfer control information unit. (Tezuka, col. 8, 43-47). Furthermore, Tezuka describes an empty buffer count that indicates the number of empty buffers in a common buffer (Tezuka, col. 12, ll. 42-47). The empty buffer count is stored in a discrete empty buffer pointer not in each one of a plurality of storage elements used to store packet data. (Tezuka, col. 12, ll. 48-51). Moreover, Tezuka describes that a designated number of buffers set in the release count designation unit can be released to a common buffer. (Tezuka, col. 6, ll. 18-23). Thus, the release count designation unit stores a number of the amount of buffers to be released to be used by a common buffer.

Therefore, Tezuka describes count values used to indicate and release a number of buffers used within a discrete or common buffer space and do not indicate the number of times a packet is transmitted or should be transmitted. Moreover, the buffer count, the empty buffer count, and the buffer count used by the release count designation unit are not stored within each one of said plurality of storage elements storing a plurality of packet data. Therefore, Tezuka fails to describe maintaining a transmit count value of each one of said plurality of storage maintaining a transmit count value of each one of said plurality of storage elements stored within each one of said plurality of storage elements storing a plurality of packet data.

Because Basso and Tezuka fail to describe or suggest maintaining a transmit

count value of each one of said plurality of storage elements stored within each one of said plurality of storage elements storing a plurality of packet data, the combination fails to describe the limitation. As such the combination fails to render the claim obvious.

Claims 42-46

Applicants respectfully submit that claims 42-46 are dependent directly or indirectly on claim 41, thus include the same limitations as claim 41. As such, claims 42-46 are patentable for at least the same reasons as claim 41.

Claims 11, 17 and 24

Applicants respectfully disagree with the rejection because the combination of Basso, Tezuka, and Gulick fails to describe or suggest each and every element of claims 11, 17, and 24. Applicants request reconsideration of the rejected claims.

Claims 11, 17, and 24 require an input module to store packet data within a storage element and to initialize a transmit count value of said storage element stored within said storage element. Furthermore, claims 11, 17, and 24 require a processing element to determine a release count value and to store said release count value within said storage element.

For similar reasons as discussed above, Basso and Tezuka fail to describe or suggest an input module to store packet data within a storage element and to initialize a transmit count value of said storage element stored within said storage element as required by claims 11, 17, and 24.

Gulick describes a dual port timing controller (DPTC) in conjunction with an interprocessor communication register provides a shared random access memory (S-RAM). (Gulick, Abstract). The S-RAM can be accessed either by a local processor or a host processor which in a preferred configuration, controls an integrated circuit integrated services data protocol controller. (Gulick, Abstract). The DPTC provides control signals allowing an ordinary RAM to be operated as an S-RAM. (Gulick, Abstract).

Therefore Gulick fails to describe or suggest an input module to store packet data within a storage element and to initialize a transmit count value of said storage element stored within said storage element as required by claims 11, 17, and 24.

Because Basso, Tezuka, and Gulick all fail to describe an input module to store packet data within a storage element and to initialize a transmit count value of said storage element stored within said storage element as required by claims 11, 17, and 24, the combination fails to describe or suggest the limitation. As such, the combination fails to describe each and every element of claims 11, 17, and 24, thus the combination fails to render claims 11, 17, and 24 obvious.

Claims 12-16

Applicants respectfully submit that claims 12-16 are dependent directly or indirectly on claim 11, thus include the same limitations as claim 11. As such, claims 12-16 are patentable for at least the same reasons as claim 11.

Claims 18-23

Applicants respectfully submit that claims 18-23 are dependent directly or indirectly on claim 17, thus include the same limitations as claim 17. As such, claims 18-23 are patentable for at least the same reasons as claim 17.

Claims 25-30

Applicants respectfully submit that claims 25-30 are dependent directly or indirectly on claim 24, thus include the same limitations as claim 24. As such, claims 25-30 are patentable for at least the same reasons as claim 24.

Conclusion

In view of the foregoing remarks and amendments, it is respectfully submitted that the present application is in condition for allowance.

Invitation for a telephone interview

The Examiner is invited to call the undersigned at 408-720-8300 if there remains any issue with allowance of this case.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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